

## BQ25170: 800-mA Linear Battery Charger for 1-Cell Li-Ion, and LiFePO<sub>4</sub>

### 1 Features

- Input voltage up-to 30-V tolerant
- Automatic Sleep Mode for low power consumption
  - 0.5µA (TBD) Battery leakage current
  - 85µA (TBD) Input leakage current when charge disabled
- Supports 1 cell Li-Ion, Li-Poly, and LiFePO<sub>4</sub>
- External resistor programmable operation
  - VSET to Set battery regulation voltage:
    - Li-Ion: 4.05V, 4.1V, 4.2V, 4.35V, 4.4V
    - LiFePO<sub>4</sub>: 3.5V, 3.6V, 3.7V
  - ISET to Set charge current from 10mA to 800mA
- High accuracy
  - ±1% (TBD) Charge voltage accuracy
  - ±10% (TBD) Charge current accuracy
- Charging features
  - Precharge current 20% of ISET
  - Termination current 10% of ISET
  - NTC Thermistor input to monitor battery temperature
  - TS Pin for charger control
  - Open-drain output for status and fault indication
  - Open-drain output for power good indication
- Integrated fault protection
  - 6.6V (TBD) IN Over-voltage protection
  - VSET Based OUT over-voltage protection
  - 1000mA (TBD) Over-current protection
  - 125°C (TBD) Thermal regulation; 150°C (TBD) Thermal shutdown protection
  - OUT Short-circuit protection
  - VSET, ISET Pins short/open protection

### 2 Applications

- True Wireless Headsets
- Wearable Accessories, Smart Band
- Beauty & Grooming
- Electric Toothbrush
- Fleet Management, Asset Tracking

### 3 Description

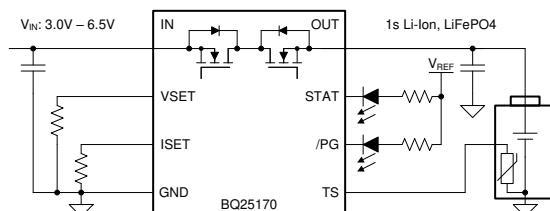
The BQ25170 is an integrated 800mA linear charger for 1-cell Li-Ion, Li-Polymer, and LiFePO<sub>4</sub>. The device has a single power output that charges the battery. The system load can be placed in parallel with the battery, as long as the average system load does not prevent the battery from charging fully within the safety timer duration. When the system load is placed in parallel with the battery, the charge current is shared between the system and the battery.

The device has three phases of charging: pre-charge to recover a fully discharged battery, fast-charge constant current to supply the bulk of the charge, and voltage regulation to reach full capacity. In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if an internal temperature threshold,  $T_{REG}$ , is exceeded.

### Device Information

PART NUMBER <sup>(1)</sup>	PACKAGE	BODY SIZE (NOM)
BQ25170	WSON (8)	2.0 mm x 2.0 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



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## 4 Device and Documentation Support

### 4.1 Device Support

#### 4.1.1 Third-Party Products Disclaimer

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#### 4.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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#### 4.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 4.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 5 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## 5.1 Package Option Addendum

### Packaging Information

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish <sup>(6)</sup>	MSL Peak Temp <sup>(3)</sup>	Op Temp (°C)	Device Marking <sup>(4) (5)</sup>
PQ25170DSGT	PREVIEW	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	P17X

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PRE\_PROD** Unannounced device, not in production, not available for mass market, nor on the web, samples not available.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

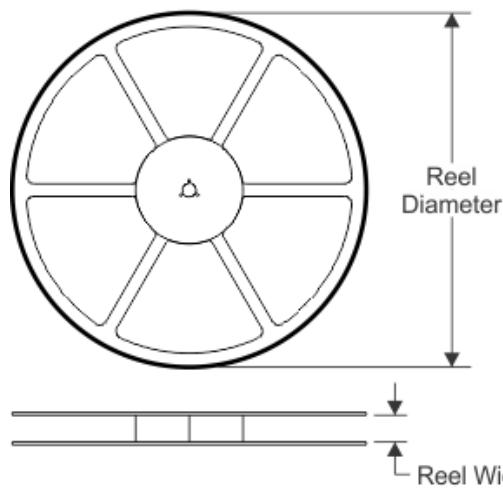
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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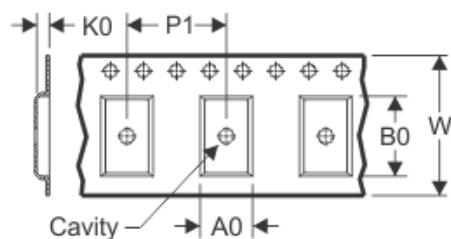
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## 5.2 Tape and Reel Information

### REEL DIMENSIONS

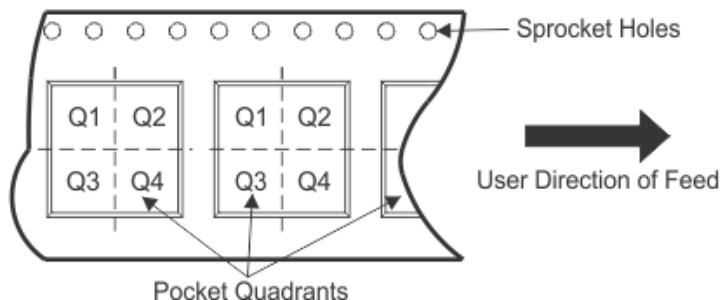


### TAPE DIMENSIONS



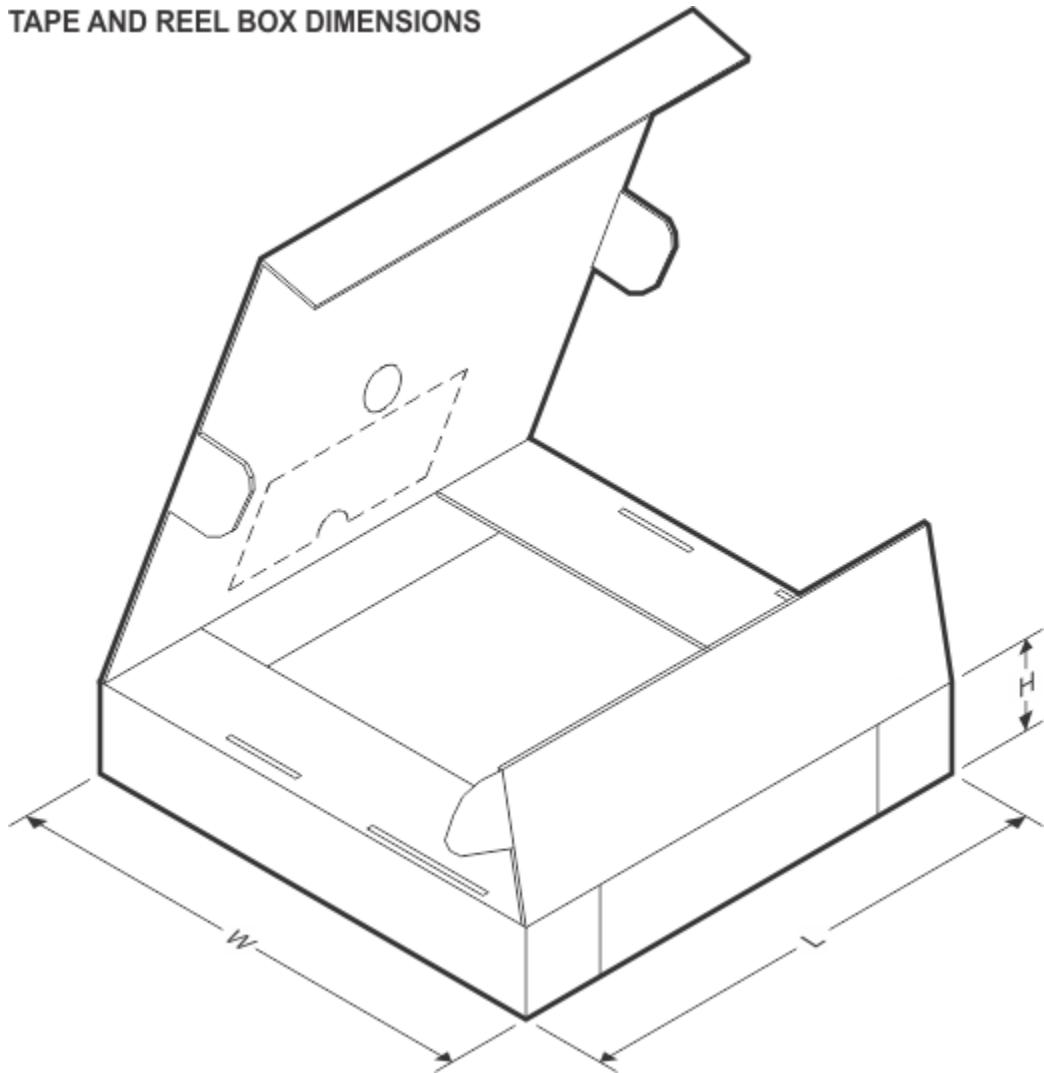
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PQ25170DSGT	WSON	DSG	8	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2

## TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PQ25170DSGT	WSON	DSG	8	250	205.0	200.0	33.0

## 5.3 Mechanical Data

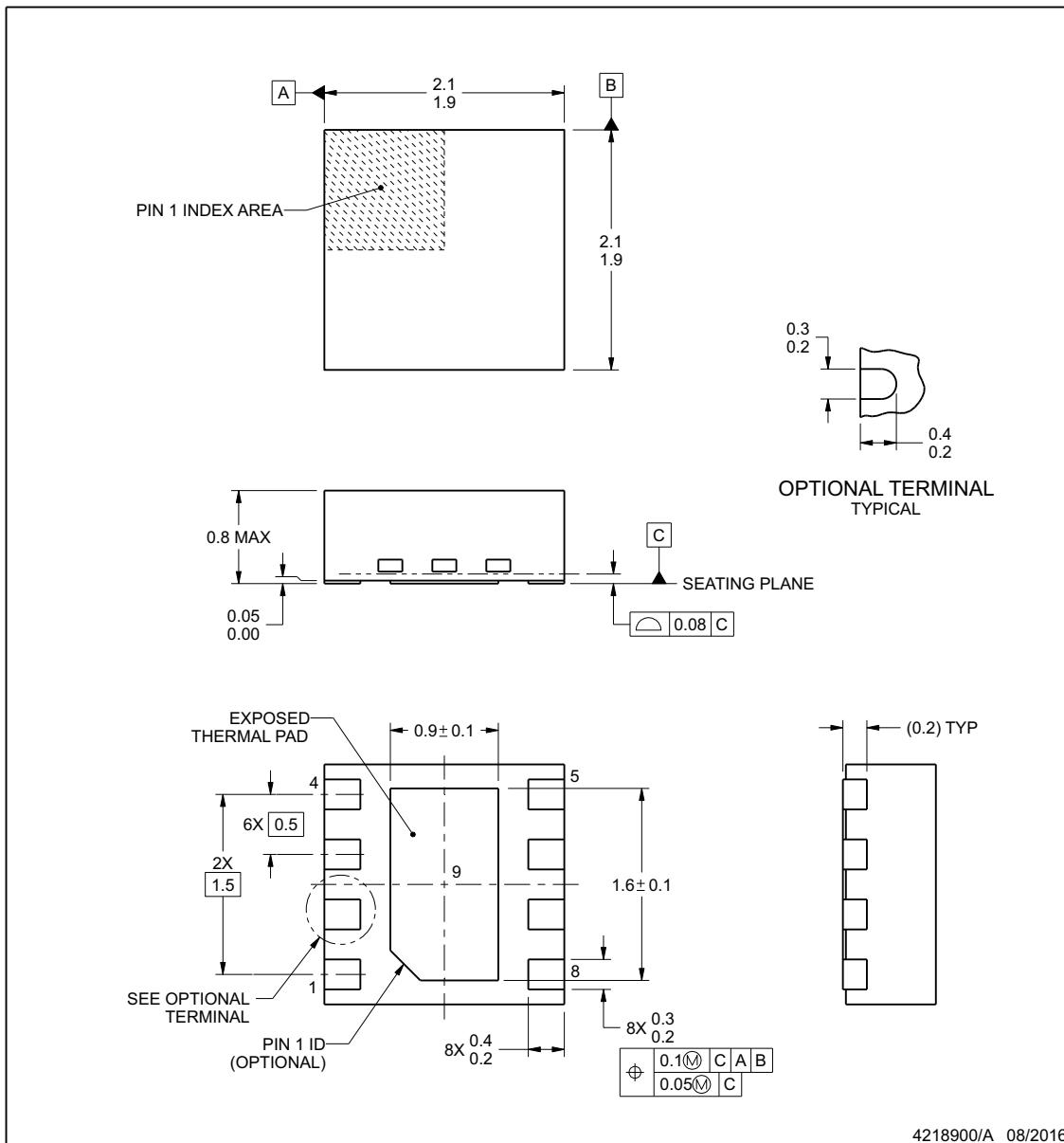
### DSG0008A



### PACKAGE OUTLINE

#### WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



#### NOTES:

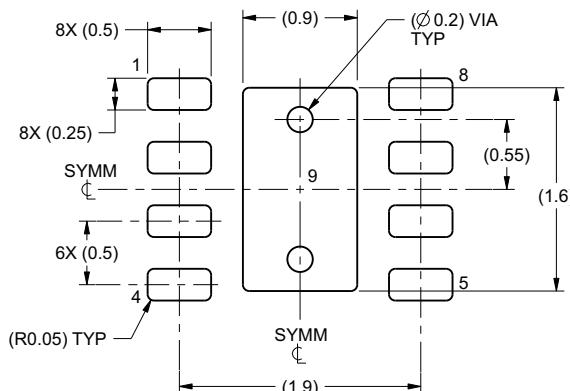
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

## EXAMPLE BOARD LAYOUT

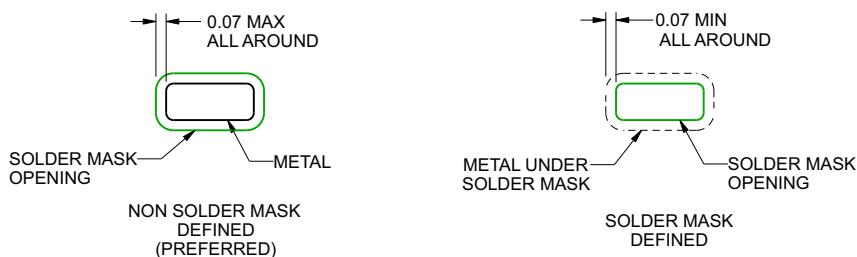
**DSG0008A**

## WSON - 0.8 mm max height

## PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:20X



## SOLDER MASK DETAILS

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#### NOTES: (continued)

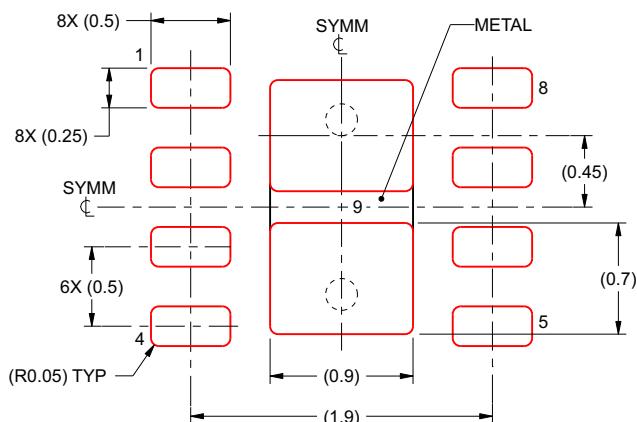
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

## EXAMPLE STENCIL DESIGN

**DSG0008A**

**WSON - 0.8 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



4218900/A 08/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

**ADVANCE INFORMATION**

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